



# G S NITESH NARAYANA

Barcelona ◊ Spain

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## VISION

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To work in world-class industry teams, solving challenging real-world problems using computer architecture.

### Current Requirements

- Actively seeking a full time opportunity within industry research and product teams focused on, but not limited to, Efficient architectures and Heterogeneous/Hybrid architectures.

## EDUCATION

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### Universitat Politècnica de Catalunya- UPC Barcelona

2024-Present

PhD in Computer Architecture

Advised by: Prof. Abhijit Das (IIT Hyderabad),

Dr. Sanyam Mehta (Oasis Software and Research,USA) and Prof. Xavier Martorell (BSC,UPC)

### Indian Institute of Information Technology Design and Manufacturing Kancheepuram, Tamil Nadu, India

2016-2021

B.Tech in Computer Engineering + M.Tech in Computer Engineering

CGPA 9.22 (with Distinction, Ranked among Top 5 in class)

### Delhi Public School Hyderabad

2003-2016

Class-12 Percentage: 93.2 ; Class-10 CGPA: 10/10

## PUBLICATIONS (SELECTED)

Full list → [nitesh.contact/publication](http://nitesh.contact/publication)

1. **Nitesh Narayana GS**, Sonam Sonam, and Xavier Martorell. “AutoTune-TCU: Hardware-Software Co-Design of a Learning-Based Self-Optimizing TCU for HPC”. in: *10th Workshop on Cognitive Architectures (CogArch), co-located with ISCA. 2026*
2. Mohammad Nasser, **Nitesh Narayana GS**, Abhijit Das, and Debiprasanna Sahoo. “Juggler: A Dynamic Warp Scheduler for GPGPUs”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2026), pp. 1–1
3. **Nitesh Narayana GS** and Xavier Martorell. “One-for-All Chip: Same, Similar, Different — What You Want, When You Want It, All in One Chip”. In: *Wild and Crazy Ideas (WACI) Session in ASPLOS 2025*
4. **Nitesh Narayana GS** and Abhijit Das. “Apparate: Evading Memory Hierarchy with GodSpeed Wireless-on-Chip”. In: *Wild and Crazy Ideas (WACI) Session in ASPLOS 2024*
5. **Nitesh Narayana GS**, Marc Ordoñez, Lokananda Hari, Franyell Silfa, and Antonio González. “ReuseSense: With Great Reuse Comes Greater Efficiency; Effectively Employing Computation Reuse on General-Purpose CPUs”. In: *arXiv preprint arXiv:2311.10487. 2023*
6. **Nitesh Narayana GS**, Franyell Silfa, and Antonio González. “Characterizing DNN Workloads on General Purpose CPUs”. In: *ACACES 2022: Poster Abstracts. 2022*, pp. 27–31

## EXPERIENCE

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### Senior Research Engineer (RE3)

June 2025 - Present

*Computer Architecture for Parallel Paradigms Group*      *Barcelona Supercomputing Center - Barcelona, Spain*

- Proposing architectures for latest RISC-V Integrated, Vector Matrix Extensions for Cores and Vector Processors along with Microscaling instruction integration.
- Benchmarking and profiling of floating point riscv applications.
- Actively contributing to the development of chips under the DARE Project, a European Supercomputer chip initiative.
- Guiding and mentoring students in their research projects.
- Collaborating in research projects with other groups in the center.

### SD Research Engineer 1

November 2024 - April 2025

*RADICAL Group (RAD Team)*

*AMD-Xilinx Research - Dublin, Ireland*

- Explored advanced branch prediction strategies for future AMD Zen core architectures.
- Implemented and upgraded in-house tools and simulators for steadfast research to product idea conversion.

### Research Assistant

October 2021 - August 2024

*Investigator under CoCoUnit ERC Grant, ARCO Research Group*

*UPC Barcelona - Barcelona, Spain*

- Implemented ARM SVE instructions for official gem5 main repo (to be merged in next release)
- Enhancing performance and energy efficiency of general-purpose CPUs for specialized workloads, with emphasis on vector units.
- Conducted in-depth analysis and characterization of Cognitive workloads with a focus on ARM SVE vector extension support. Developed workloads utilizing ARM-NN and Compute Library.
- Designed and implemented vector extensions and special units for ARM CPUs, contributing to the advancement of processor capabilities.
- Mentored and supervised a Bachelor's student in Computer Science, providing guidance and support throughout their research project.

### Research Intern

June 2021 - August 2021

*Researcher, CAIRN/TARAN Team*

*IRISA - INRIA, Rennes - Bretagne Atlantique, France*

- Worked on design space exploration for LSTM accelerators on FPGA/DPU using Vitis AI / HLS frameworks.

### Co-Op Engineer

August 2020 - July 2021

*Core Performance Team (Zen-Team)*

*AMD, India Private Limited, Bangalore*

- Designed a fast simulation paradigm for AMD's in-house cycle accurate core simulator, enhancing the efficiency of simulation processes.
- Conducted workload characterization to extract cacheline-level information for value prediction and identified potential optimizations.
- Developed a comprehensive verification environment and strategies for AMD's next-generation cache organization, ensuring the robustness and effectiveness of the design.
- Benchmarked and compared GPU performance under machine learning workloads, providing valuable insights for performance optimization and decision-making.

### Research Intern

July 2019 - July 2021

*Researcher*

*IIT, Madras*

- Collaborated with Prof. Madhumutyam to tackle challenges related to Prefetching in SSDs and Value Prediction, contributing to advancements in performance.
- Developed a simulator for Deep Learning Accelerator as part of a project supervised by Prof. Pratyush Kumar at RISE Labs

- Conducted research on DRAMs, memory devices, and controllers, exploring topics such as refresh rates and data persistence using FPGAs. Utilized various simulators to analyze and understand different metrics under the guidance of Prof. V. Kamakoti and Prof. Chester Rebeiro.

**Project Intern @ Shakti Team RISE Labs**

May 2019 - July 2019

*Researcher*

*IIT, Madras*

- Designed DUT interface integrated with Spike simulator for Verification of Shakti RISC-V Processor. Worked on other RISC-V based simulators.

**Research Assistant @ HPRCSE Lab**

December 2018 - July 2020

*Researcher and Lab Incharge*

*IIITDM, Kancheepuram*

- Conducted research on various topics in Computer Organization & Architecture and Network Systems, including Circuit Obfuscation, Branch Prediction, and Hardware Packet Classification.
- Mentored student projects, providing guidance and support for research and development.
- Served as a resource person for lab workshops, sharing expertise to enhance participants' understanding of relevant topics.
- Managed and supervised winter break interns, fostering their professional growth and aligning their contributions with project objectives.

**CavinTek, Sand-Box Program**

December 2017 - January 2018

*GUI Developer*

*MadeIT, IIITDM Kancheepuram*

- Project: Automated Physical File Tracking System for CavinTek under MadeIT
- Headed the design and development of the Software Design team for the project. Developed the API in Visual Studio with SQL Server as the back-end.

## TALKS

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**Design Thinking and Thinking Design Workshop**

September 2019

*Resource Person and Organizer*

*Delhi Public School, Hyderabad*

- Conducted a workshop, for class XI Students, dealt with shining light on unorthodox thinking methodologies for solving real world problems.

**High Performance Computing Workshop by HPRCSE**

December 2018,2019

*Resource Person*

*IIITDM, Kancheepuram*

- Annually conduct workshop on HPC, give lectures on Code Profiling(GProf, LIKWID, Valgrind,Intel VTune) and CUDA programming, Nvidia architectures.

## TEACHING EXPERIENCE

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**Advanced Computer Organization and Architecture Lab**

Fall 2019, 2020, 2022, Winter 2025, 2026

*TA/LA*

*IIT, Madras*

- Served as a teaching assistant for the course Advanced Computer Organization and Architecture with Lab under Dr. Madhumutyam(Professor of Computer Science Department, PACE Labs). Assisted students in understanding concepts related to ARM, x86, and RISC-V assembly, covering multiple versions of the course.

**Computational Engineering LAB**

January 2018 - April 2018

*TA/LA*

*IIITDM, Kancheepuram*

- Worked as the LAB Assistant during SEM-4 under Dr.N.Sadagopan (Assistant Professor of Computer Science and HOD).

## CERTIFICATES AND GRANTS

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|---|--|
| <b>EPO Patent Course 1</b><br><i>Create-Protect-Innovate Bringing Ideas to Market</i> | December 2025<br><i>Barcelona, Spain</i> |
| <b>DATE 2024</b><br><i>Young Peoples Program Full Grant</i>                           | March 2024<br><i>Valencia, Spain</i>     |
| <b>ACACES HIPEAC Summer School 2022</b><br><i>Attendance Grant</i>                    | June 2022<br><i>Fiuggi, Italy</i>        |
| <b>CoDS COMAD 2020</b><br><i>Attendance and Travel Grant</i>                          | Jan 2020<br><i>Hyderabad, India</i>      |
| <b>Foundations of Computer Systems Design (NPTEL)</b><br><i>All India Rank 1</i>      | 2018-2019<br><i>India</i>                |

## POSITIONS OF RESPONSIBILITY

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### PC Member (Artifact Evaluation)

- ASPLOS 2025; HPCA 2025, 2024; ISCA 2024; PACT 2024

### Organizing Team

- RISC-V Summit 2023 (Barcelona, Spain), MATEO 2022 Workshop (Barcelona, Spain)

### CS Club

*Head Core(since August) & Resource Person*

January 2019 - June 2020

*IIITDM, Kancheepuram*

- Headed the club core team and ran learning sessions on systems, architecture, and programming topics.

## TECHNICAL STRENGTHS

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|------------------------------|--|
| <b>Programming Languages</b> | ARM Assembly, C/C++, Python, Verilog, x86  |
| <b>Tools &amp; Packages</b>  | gem5, ARM-NN and Compute Library, McPat, Cacti, Vitis HLS and AI, Pytorch, TensorFlow, Git, CI/CD, CoCoTB, AutoCAD |

## INTERESTS

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|---------------------------|--|
| <b>Research Interests</b> | Computer Hardware, Domain Specific Architectures, Parallel Computer Architecture, Sustainable Computing  |
| <b>Others</b>             | Design Thinking, Problem Solving, Teaching, Writing, Poetry<br>Physics and Biology, Space Science, Music, Sketching<br>Quantum Computation and Exploring New Domains |

## LANGUAGES

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| <b>Expert</b>  | English, Telugu, Hindi |
| <b>Learner</b> | Spanish, Tamil         |

## REFERENCES

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|-------------------------------|--|
| <b>Prof. Xavier Martorell</b> | Barcelona Supercomputing Center (BSC), xavier.martorell@bsc.es |
| <b>Dr. Sanyam Mehta</b>       | Oasis Software and Research, USA, sanyam.mehta@gmail.com       |
| <b>Prof. Abhijit Das</b>      | IIT Hyderabad, abhijit.das@cse.iith.ac.in                      |